

# NTMS4706N

## Power MOSFET

30 V, 10.3 A, Single N-Channel, SO-8

### Features

- Low  $R_{DS(on)}$
- Low Gate Charge
- Standard SO-8 Single Package
- Pb-Free Package is Available

### Applications

- Notebooks, Graphics Cards
- Synchronous Rectification
- High Side Switch
- DC-DC Converters

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	30	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	8.6	A
		$T_A = 85^\circ\text{C}$		6.2	
	$t \leq 10\text{ s}$	$T_A = 25^\circ\text{C}$		10.3	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	1.5	W
		$t \leq 10\text{ s}$		2.2	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	6.4	A
		$T_A = 85^\circ\text{C}$		4.6	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	$P_D$	0.83	W
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$		$I_{DM}$	31	A
Operating Junction and Storage Temperature			$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)			$I_S$	2.1	A
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 25\text{ V}, V_{GS} = 10\text{ V}, I_L\text{ Peak} = 7.5\text{ A}, L = 10\text{ mH}, R_G = 25\ \Omega$ )			$E_{AS}$	150	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^\circ\text{C}$

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	83.5	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	58	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	150	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surfaced mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surfaced mounted on FR4 board using the minimum recommended pad size.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

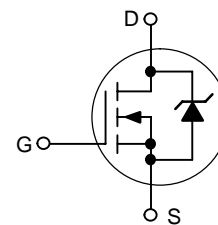


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<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	$I_D$ MAX (Note 1)
30 V	9.0 m $\Omega$ @ 10 V	10.3 A
	11.4 m $\Omega$ @ 4.5 V	

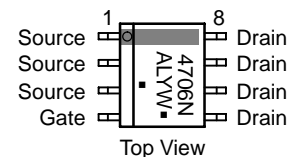
### N-Channel



### MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8  
CASE 751  
STYLE 12



4706N = Device Code  
A = Assembly Location  
L = WaferLot  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTMS4706NR2	SO-8	2500/Tape & Reel
NTMS4706NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			21		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 125°C		50	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0		2.5	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-4.8		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10.3 A		9.0	12	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		11.4	15	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		19		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 24 V		950		pF
Output Capacitance	C <sub>oss</sub>			400		
Reverse Transfer Capacitance	C <sub>rss</sub>			100		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		10	15	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.25		
Gate-to-Source Charge	Q <sub>GS</sub>			2.4		
Gate-to-Drain Charge	Q <sub>GD</sub>			4.5		
Gate Resistance	R <sub>G</sub>			1.82		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 15 V, I <sub>D</sub> = 1.0 A, R <sub>G</sub> = 3.0 Ω		7.5	12	ns
Rise Time	t <sub>r</sub>			4.0	8.0	
Turn-Off Delay Time	t <sub>d(off)</sub>			24	40	
Fall Time	t <sub>f</sub>			14	25	

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.1 A	T <sub>J</sub> = 25°C	0.74	1.0	V
			T <sub>J</sub> = 125°C	0.57		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 2.1 A		34		ns
Charge Time	t <sub>a</sub>			16		
Discharge Time	t <sub>b</sub>			18		
Reverse Recovery Charge	Q <sub>RR</sub>			29		

3. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

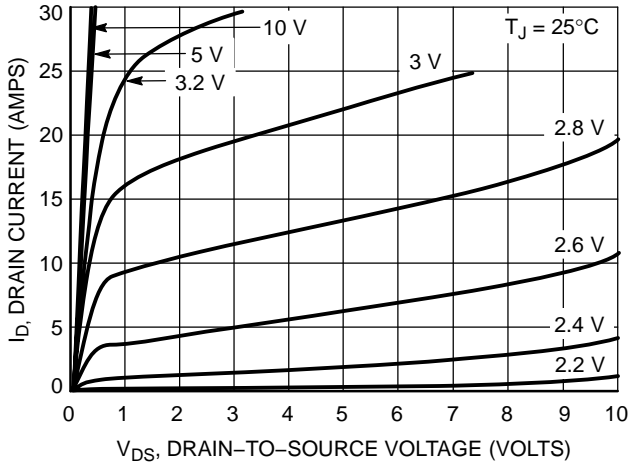


Figure 1. On-Region Characteristics

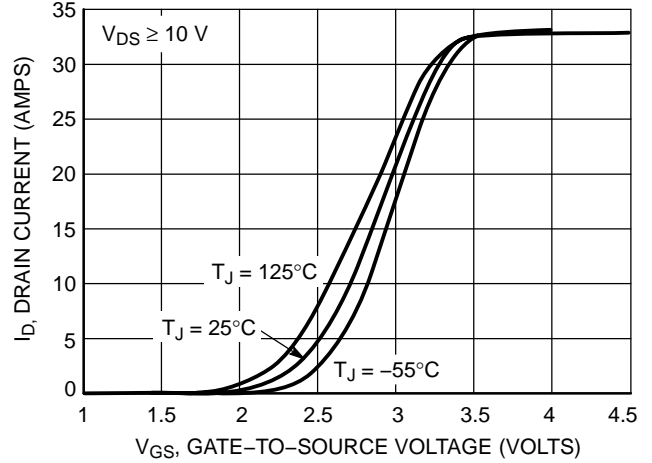


Figure 2. Transfer Characteristics

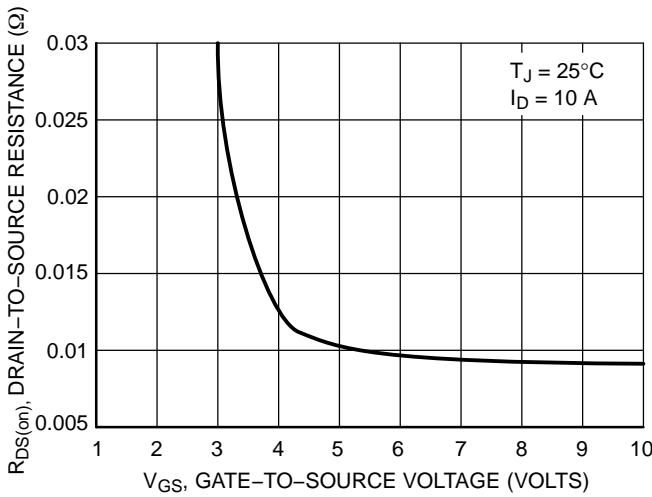


Figure 3. On-Resistance vs. Gate-to-Source Voltage

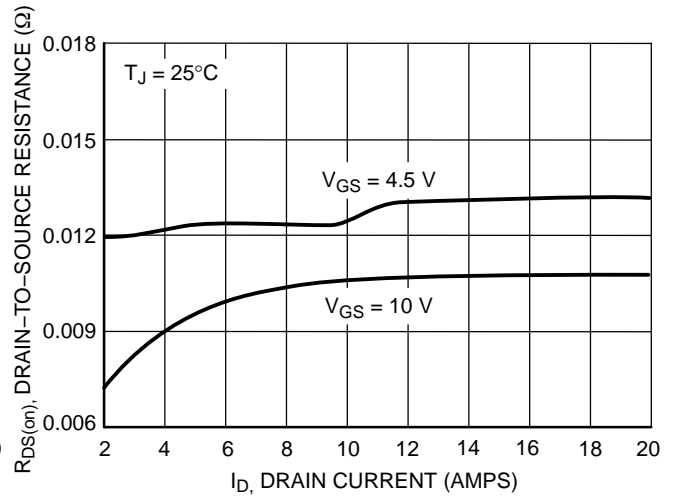


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

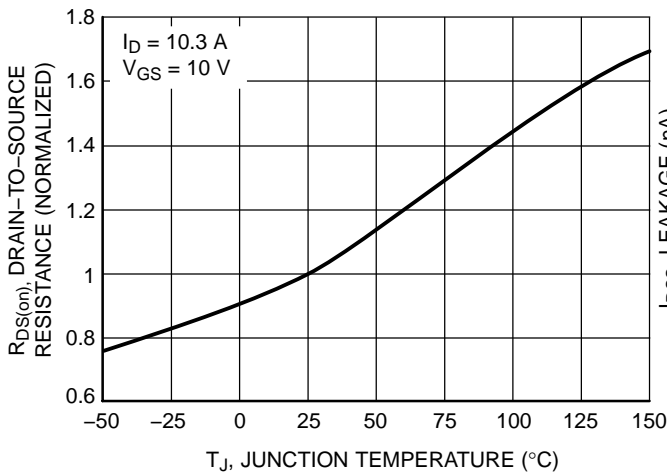


Figure 5. On-Resistance Variation with Temperature

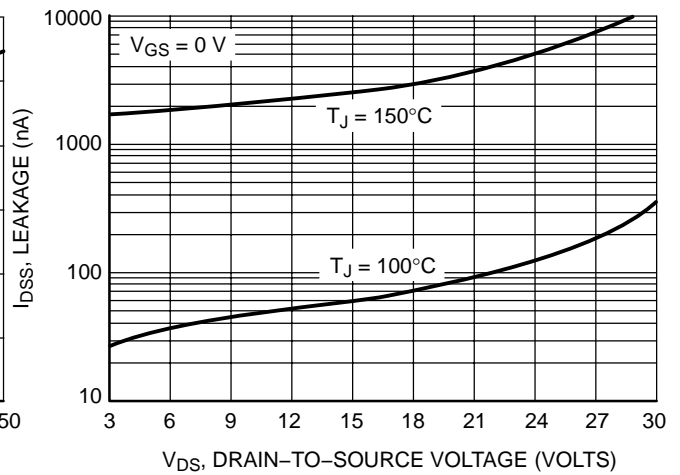


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL PERFORMANCE CURVES

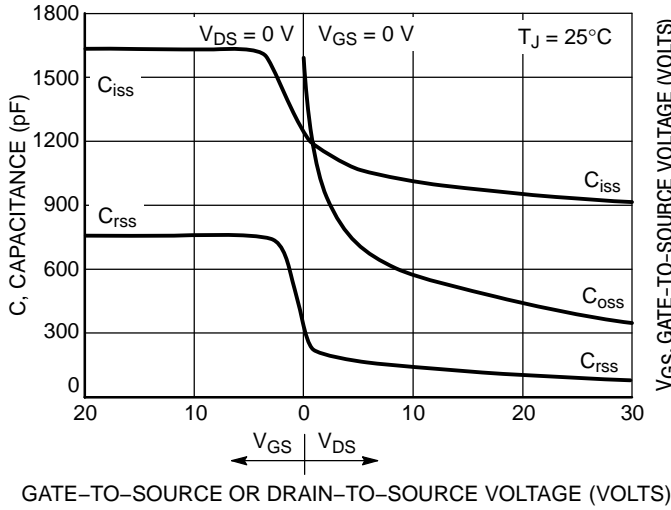


Figure 7. Capacitance Variation

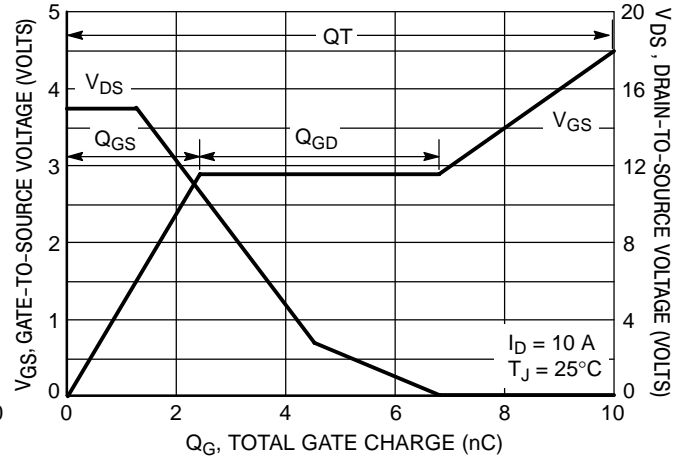


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

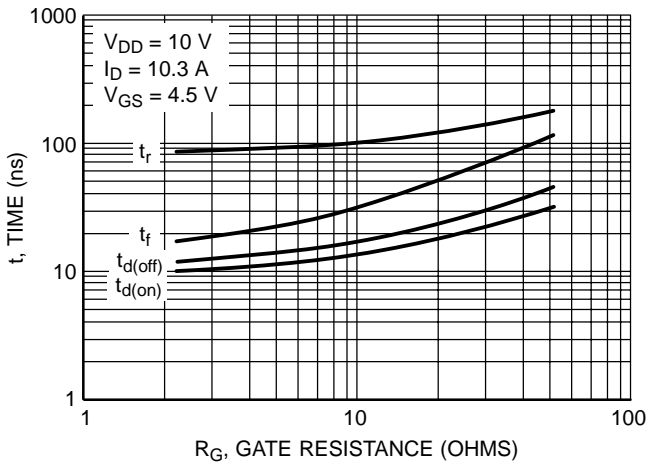


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

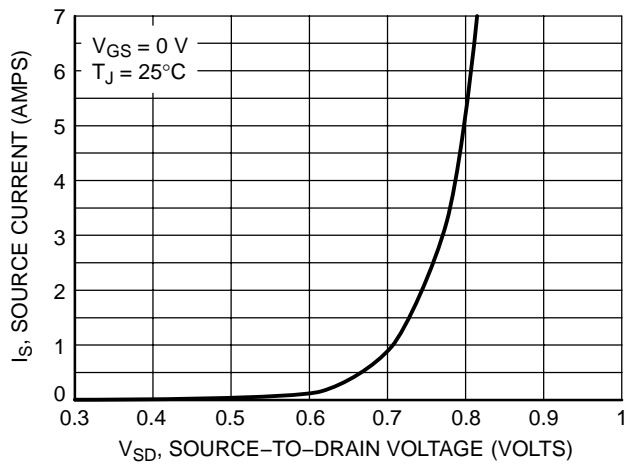
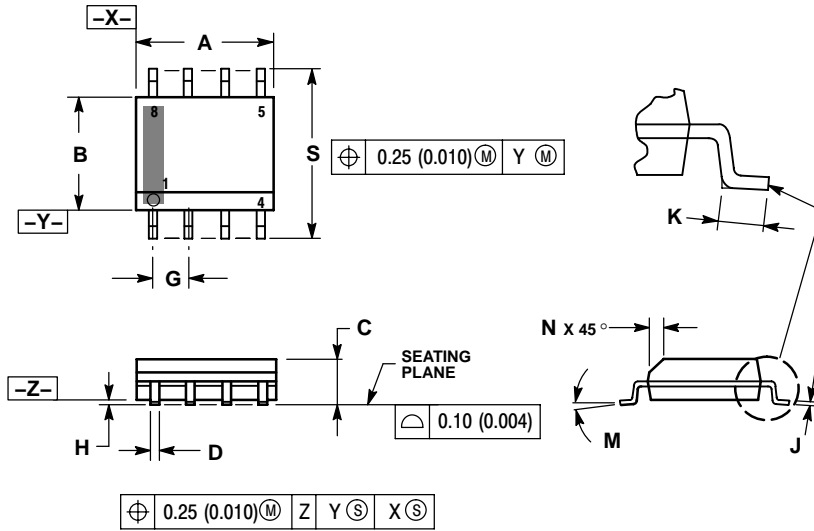


Figure 10. Diode Forward Voltage vs. Current

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## PACKAGE DIMENSIONS

SOIC-8  
CASE 751-07  
ISSUE AG



### NOTES:

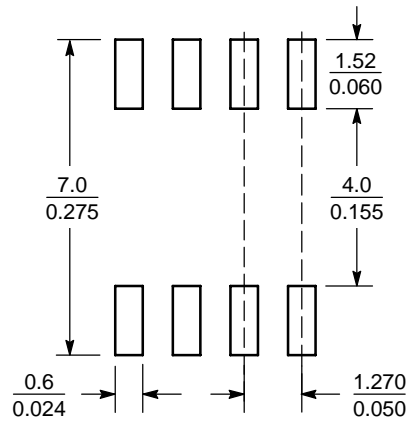
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### STYLE 12:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

### SOLDERING FOOTPRINT\*



SCALE 6:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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